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U.S. PATENT APPLICATION

FOR

ETCHING PROCESS FOR ORGANIC ANTI-REFLECTIVE COATING

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ETCHING PROCESS FOR ORGANIC ANTI-REFLECTIVE COATING

Field of the Invention

The present invention relates to an improved method for etching organic anti-reflective coatings (ACR's) in the fabrication of integrated circuits.

Background of the Invention

Electronic, solid state microchips such as those in computer microprocessors, hold thousands of individual systems each of which is made up of thousands of individual electronic components such as transistors, resistors, and capacitors. The manufacture of solid state electronic devices relies on assembling layers of semiconducting, conducting, and insulating materials in precise patterns and uniform thicknesses, selectively etched to create electronic components and systems according to the functions desired. Because the components and systems are all made into one chip, or substrate, and interconnected, these circuits are appropriately termed "integrated circuits."

The production of integrated circuits is highly competitive. Therefore improving the efficiency of the manufacturing steps means a competitive advantage. Typically, the production of integrated circuits requires fabricating one or more networks of conductive pathways interconnecting the components to form systems and interconnecting the systems to form circuits. An important manufacturing step is the formation of a network of conducting pathways, or interconnecting network, over a semiconducting substrate *via* photolithography and etching (collective these processes are referred to "patterning"). This is typically accomplished by coating a conductive, metallic layer, with a light sensitive coating, *i.e.*, a photoresist coating ("photoresist"). The photoresist is then exposed to actinic light through a mask which blocks the light in a pattern corresponding to the pattern desired for the conducting interconnecting network.

The photoresist coating is subsequently "developed," that is, the parts of the photoresist coating which were exposed to the actinic light are selectively removed, thereby exposing the conductive surface below in a pattern corresponding to the openings in the mask. Usually the exposed metal layer is removed by plasma etching, but may also be removed by wet chemical etching, leaving the desired interconnecting network.

The demand in recent years for greater miniaturization of integrated circuits has led to increased circuit density, which requires shorter wavelength light such as deep ultraviolet(UV) to expose the photoresist. While the short wavelength light theoretically should yield exposures of high resolution, unfortunately it tends to reflect off the metallic layer back through the photoresist layer. This reflection sets up interference with the incoming light which reduces resolution. A discussion of this phenomenon can be found in *Silicon Processing for the VLSI Era*, S. Wolf, *et al.*, v. 1, "Process Technology," Lattice Press, Sunset Beach, CA (1987). To solve this problem, an anti-reflective coating (ARC) is typically deposited on the metallic layer before the photoresist layer to reduce the unwanted reflection and consequential loss of resolution. The ARC's widely used in the integrated circuit industry are polyimides although other organic anti-reflective material can be used.

After the photoresist has been exposed to UV and developed, the ARC must be removed by etching to uncover the underlying conductive, metallic layer or coating. The prior art teaches that this may be done by plasma etching. However, a system of etching agents and conditions must be used which effectively etch away the ARC but leave the photoresist relatively intact.

U.S. Patent No. 5,655,110, "*Krivokapic et al.,*" incorporated herein by reference, discusses the importance of maintaining critical dimensions during etching operations in mass produced semiconductor wafers. U.S. Patent No. 5,126,289, "*Ziger,*" teaches a method of etching the photoresist layer and the underlying aluminum layer in one operation using ionized carbon tetrachloride as the etching agent. However, *Ziger* is silent regarding degradation of the photoresist.

Thuy B. Ta in U.S. Patent No. 5,308,742 ("*Ta*"), incorporated herein by reference, claims a method of manufacturing an integrated circuit which includes a step of plasma etching a polyimide ARC using trifluoromethane (CHF_3) and elemental oxygen (O_2) with argon as a carrier gas. This patent asserts that CHF_3 promotes polymer formation while the argon acts as a sputter component which removes the polymer formed by CHF_3. The sputter component travels primarily in a vertical direction so that the polymeric material on the sidewalls of the interconnecting network etched through the photoresist is not removed. This protects the sidewalls of the photoresist from lateral attack by oxygen. Purportedly, this method provides critical dimension control because it is selective for the ARC.

In *Ta*, oxygen appears to be the actual etching agent. Oxygen is an aggressive oxidizing agent and tends to be non-specific and detrimental to some solid state components. A milder oxidizing agent would offer greater selectivity between the ARC and the photoresist, and hence, an improvement over the process of *Ta*. Selectivity is important because the CHF_3 would not provide protection in the vertical direction if Ar sputtering removes CHF_3 deposited on top of the photoresist. Excessive erosion impairs the photoresist's masking properties during the etching of the ARC and/or underlying conductive coating.

We have found an improved process for selectively and effectively removing an ARC without the use of oxygen, thus, reducing degradation of the photoresist.

Summary of the Invention

A first aspect of the present invention is a process for etching an organic ARC on a metallic substrate comprising exposing the ARC to a system of etching agents in an ionized state in a reaction chamber of a plasma generating device, the system of etching agents including one or more fluorine-containing compounds, an inert carrier and chlorine. This process is particularly useful for preserving the critical dimensions of a photoresist while removing exposed areas of an organic ARC during the manufacturing of an integrated circuit.

A second aspect is a formulation of one or more fluorine-containing compounds, an inert carrier gas and chlorine which is employed in the process of the first aspect. In one embodiment of the formulation, the fluorine-containing compound is selected from the group consisting of CF_4, CHF_3, C_2F_6, CH_2F_2, SF_6, C_nF_{n+4}. In a particular embodiment the fluorine-containing compound is CHF_3 and the inert carrier is argon.

Brief Description of the Drawings

Fig. 1a is a schematic, perspective view of a portion of a semiconductor composite chip after the photoresist coating has been etched but before the ARC has been removed.

Fig. 1b is a schematic cross sectional view of the portion of the chip shown in Fig. 1a.

Fig. 2 is a view similar to Fig. 1a. after the ARC has been removed by a process using O_2..

Fig. 3 is a view similar to Fig. 1a. after the ARC has been removed by the process of the present invention.

FIG. 4 is a schematic view of a high density plasma ECR reactor which can be used to carry out the process according to the invention.

FIG. 5 is a schematic of a high density plasma TCP™ reactor which can be used to carry out the process according to the invention.

Detailed Description of the Preferred Embodiments

Referring to Fig. 1a, a perspective view of a greatly magnified section of a semiconductor composite chip **10** during manufacturing after the photoresist **12** has been exposed and developed, shows the interconnecting network **14** forming the circuit pattern **15**. That is, the area of the conductive coating **16** corresponding to those portions of the photoresist not exposed, will become the network of conductive pathways interconnecting the components and systems. The conductive coating or layer covers a semiconductor base **17**. Fig. 1b, a cross sectional view corresponding to Fig. 1a, more clearly shows that after the photoresist is developed, part of the ARC **18**

covers the bottom of the interconnecting network **14**. This part of the ARC must be removed before the underlying conductive coating **16** can be removed by etching.

Note in Fig. 1a and Fig. 1b that the interconnecting network **14** formed by exposure and development of the photoresist **12** are clean and precise. However, if the system of agents used for removing the ARC at the bottom of the interconnecting network **14** attacks the non-etched parts of the photoresist **12**, the precision of the interconnecting network **14** may be seriously degraded.

In previous generations of integrated circuits, the conductive pathways formed by etching the conductive coating were relatively well separated so that some degradation of photoresist could generally be tolerated. However, in the present generation of integrated circuits, the conductive pathways are often so close together that even a small amount of degradation can be critical. Further, in order to achieve high resolution during exposure and development of deep UV photoresists, the thickness of the photoresist has been reduced from around 12000Å to around 7000 to 8000Å. This leaves less photoresist to protect the underlying layers during etching of the ARC.

Fig. 2 is a schematic illustration of the results of removing the ARC with a system of agents containing O_2 ionized in a plasma generating chamber. For example, a system which employs a mixture of O_2 and N_2. While this system of agents containing O_2 effectively removes the ~~ARC~~ they also attack the photoresist **12** causing general thinning and degradation indicated as points **20** in Fig. 2. As illustrated in Fig. 2, the degradation reduces the precision of the interconnecting network **14** and can cause undesirable exposure of the underlying layers at other locations. Because the interconnecting network **14** controls what is etched away from the conductive coating, thinning and degradation can cause voids in the conducting pathways or faulty connections leading to errors in the function of the integrated circuit.

Fig. 3 is a schematic illustration of the results of removing the ARC with a system of agents of the present invention. Note that the photoresist **12** has been only minimally affected and retains its precision pattern. Therefore, the precision pattern

will be transferred to the formation of conductive pathways in the next step when the exposed conductive coating **16** is etched away.

For the present process, the carrier gas is an inert, noble gas, preferably argon (Ar), although, other noble gases such as helium, neon, krypton, xenon or mixture thereof may be used. The source of chlorine preferably is chemically pure elemental chlorine (Cl_2). Alternatively, it is possible to use another chlorine containing gas such as HCl or BCl_3. Similarly, while CHF_3 is the preferred source of fluorine, other fluorocarbon gases or combination of such gases may be used.

FIG. 4 shows an ECR reactor 100 which can process a substrate with a high density plasma. The reactor includes a reaction chamber 102 wherein a substrate is subjected to treatment with a plasma gas. In order to generate the high density plasma, the reactor includes a plasma generating chamber 103 wherein a high density plasma is generated by the combination of microwave energy transmitted through microwave guide 104 and magnetic energy generated by electromagnetic coils 105. The high density plasma can be generated from a suitable gas or gas mixture and an ion beam is extracted from the plasma chamber through orifice 103a. If desired, the orifice 103a can have the same diameter as the chamber 103. A substrate 106 is supported on a substrate support 107 such as an electrostatic chuck having a substrate temperature controlling mechanism associated therewith.

The high density plasma generated in chamber 103 can be confined within horn 108 by electromagnetic coils 118 and directed to the substrate 106 by applying an RF bias to the substrate by means of an RF source 109 and associated circuitry 110 for impedance matching, etc. The reaction chamber 102 is evacuated by a suitable vacuum arrangement represented generally by the evacuation port 111. In order to introduce the etch reactants into the high density plasma, the horn 118 can include one or more gas injection arrangements such as gas distributing rings on the inner periphery thereof whereby reactants such as F and Cl can be introduced into the high density plasma. The reactant or reactants can be supplied through one or more passages represented generally at 112. In order to produce a plasma in plasma generating chamber 103,

argon can be introduced into the plasma generating chamber 103 by one or more passages represented generally at 113.

Microwave energy represented by arrow 114 travels through dielectric window 115 and enters the plasma generating chamber 103, the walls of which are water cooled by water supply conduit 117. Electromagnetic coils 118 below substrate holder 107 can be used for shaping the magnetic field in the vicinity of the substrate 106. A DC power source 119 provides power to the substrate holder 107 for electrostatically clamping substrate 106.

FIG. 5 shows a TCP™ reactor 120 which can process substrates with high density plasma. The reactor includes a process chamber 121 in which plasma 122 is generated adjacent substrate 123. The substrate is supported on water cooled substrate support 124 and temperature control of the substrate is achieved by supplying helium gas through conduit 125 to a space between the substrate and the substrate support. The substrate support can comprise an aluminum electrode or a ceramic material having a buried electrode therein, the electrode being powered by an RF source 126 and associated circuitry 127 for providing RF matching, etc. The temperature of the substrate during processing thereof is monitored by temperature monitoring equipment 128 attached to temperature probe 129. A similar temperature monitoring arrangement can also be used in the ECR reactor shown in FIG. 4.

In order to provide a vacuum in chamber 121, a turbo pump is connected to outlet port 130 and a pressure control valve can be used to maintain the desired vacuum pressure. Process gas containing F, Cl and an optional inert gas such as Ar can be supplied into the chamber by conduits 131, 132 which feed the reactant gases to a gas distribution ring extending around the underside of dielectric window 133. Alternatively, the process gases can be supplied through a dielectric showerhead window or other suitable gas distribution system. An inductive energy source such as an antenna in the form of a spiral TCP™ coil 134 located outside the chamber in the vicinity of the window is supplied RF power by RF source 135 and associated circuitry 136 for impedance matching, etc. When a substrate is processed in the chamber, the

RF source 135 supplies the TCP™ coil 134 with RF current at 13.56 MHz and the RF source 126 supplies the lower electrode with RF current at 400 kHz.

The present process is carried out in an ECR or TCP™ reactor of the type described above or in any suitable reaction chamber of a plasma generator. The ARC can be on a semiconductor substrate such as a semiconductor wafer, flat panel display, etc. The process may be carried out within the following window:

Pressure	--	about 0.1 to about 500 millitorr
Temperature	--	about 0° to about 100° C
Cl_2 flow	--	about 2.5 to about 200 sccm
Inert gas flow	--	0 to about 200 sccm
Fluorine containing compound gas flow	--	about 5 to about 200 sccm

preferably it is carried out within the following window:

Pressure	--	about 1 to about 100 millitorr
Temperature	--	about 30° to about 80° C
Cl_2 flow	--	about 5 to about 60 sccm
Ar flow	--	about 5 to about 80 sccm
CHF_3 flow	--	about 5 to about 80 sccm

Process time varies with the composition and proportions of the reactants, and more importantly, the thickness of the organic ARC. The end point of the process, *i.e.*, when all of the exposed ARC has been removed, can be determined by standard methods of this art using standard micro chip manufacturing equipment. For example, one may monitor an optical signal or the concentration of fluorine.

Although the present invention has been illustrated by reference to particular embodiments, those skilled in the art of integrated circuit production will appreciate variations of these embodiments may still be within the scope of the invention.